+3 Volt, Parallel-Input, Dual,12-/10-Bit DACs

Preliminary

AD7396/AD7397

FEATURES

Micro Power - 100µA/DAC
0.1µA Typical Power Shutdown
Single-Supply +2.7 to +5.5 Volt Operation
Compact 1.1mm Height TSSOP-24 Package
AD7396 – 12-bit Resolution
AD7397 – 10-bit Resolution
0.9 LSB Differential Nonlinearity Error

APPLICATIONS

Automotive 0.5 to 4.5V Output Span Voltage
Portable Communications
Digitally Controlled Calibration
PC Peripherals

GENERAL DESCRIPTION

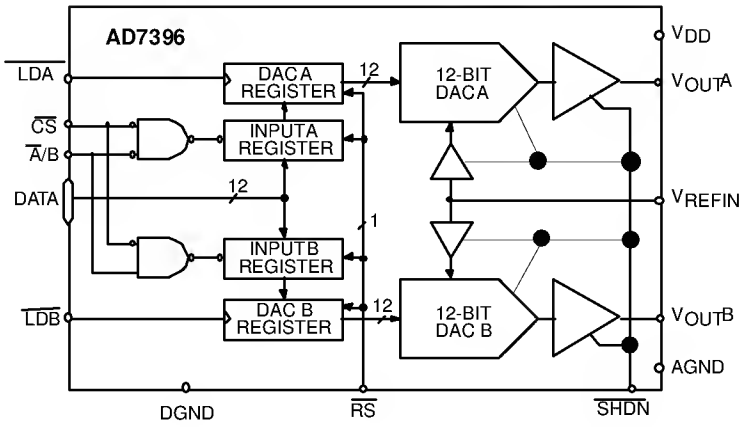
The AD7396/97 family of dual, 12 & 10-bit voltage-output digital-to-analog converters are designed to operate from a single +3 volt supply. Built using a CBCMOS process, these monolithic DACs offer the user low cost, and ease-of-use in single-supply +3 volt systems. Operation is guaranteed over the supply voltage range of +2.7 to +5.5V making this device ideal for battery operated applications.

A 12-bit wide data latch loads with a 45ns write time allowing interface to fast processors without wait states. The double-buffered input structure allows the user to load the input registers one at a time, then a single load strobe tied to both LDA+LDB inputs will update both DAC outputs simultaneously. LDA and LDB can also be activated independently to immediately update their respective DAC registers. An address input (A/B) decodes DACA or DACB when the chip select CS input is strobed. Additionally, an asynchronous RS input sets the output to zero-scale at power on or upon user demand. Power shutdown to sub microamp levels is directly controlled by the active low SHDN pin. While in the power shutdown state register data can still be changed even though the output buffer is in an open circuit state. Upon return to the normal operating state the latest data loaded in the DAC register will establish the output voltage.

Both parts are offered in the same pin out to allow users to select the amount of resolution appropriate for their applications without circuit card changes.

The AD7396/97 are specified for operation over the extended industrial (-40°C to +85°C) temperature range. The AD7397AR is specified for the -40°C to +125°C automotive temperature range. AD7396/97's are available in plastic DIP, and 24-lead SOIC packages. The AD7397ARU is available for ultra-compact applications in a thin 1.1mm height TSSOP-24 package.

FUNCTIONAL DIAGRAM



REV. 0.14

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AD7396 12-Bit ELECTRICAL CHARACTERISTICS at V_{REF}in = 2.5V, -40°C < T_A < +85°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	3V±10%	5V±10%	UNITS
STATIC PERFORMANCE					
Resolution[1]	N		12	12	Bits
Relative Accuracy[2]	INL	T_A = 25°C	±1.8	±1.8	LSB max
Relative Accuracy[2]	INL	T_A = -40°C, +85°C	±3.0	±3.0	LSB max
Differential Nonlinearity[2]	DNL	T_A = 25°C, Monotonic	±0.9	±0.9	LSB max
Differential Nonlinearity[2]	DNL	Monotonic	±1	±1	LSB max
Zero-Scale Error	V_{ZSE}	Data = 000_H, T_A = 25°C, 85°C	4.0	4.0	mV max
Zero-Scale Error	V_{ZSE}	Data = 000_H, T_A = -40°C	8.0	8.0	mV max
Full-Scale Voltage Error	V_{FSE}	T_A = 25°C, 85°C, Data = FFF_H	±8	±8	mV max
Full-Scale Voltage Error	V_{FSE}	T_A = -40°C, Data = FFF_H	±20	±20	mVmax
Full-Scale Tempco[3]	TCV_{FS}		28	28	ppm/°C typ
REFERENCE INPUT					
V_{REF}in Range	V_{REF}		$0/V_{DD}$	$0/V_{DD}$	V min/max
Input Resistance	R_{REF}		2.5	2.5	MΩ typ[4]
Input Capacitance[3]	C_{REF}		5	5	pF typ
ANALOG OUTPUT					
Output Current (source)	I_{OUT}	Data = 800_H, ΔV_{OUT} = 5LSB	1	1	mA typ
Output Current (sink)	I_{OUT}	Data = 800_H, ΔV_{OUT} = 5LSB	3	3	mA typ
Capacitive Load[3]	C_L	No Oscillation	100	100	pF typ
LOGIC INPUTS					
Logic Input Low Voltage	V_{IL}		0.5	0.8	V max
Logic Input High Voltage	V_{IH}		V_{DD}-0.6	V_{DD}-0.6	V min
Input Leakage Current	I_{IL}		10	10	µA max
Input Capacitance[3]	C_{IL}		10	10	pF max
INTERFACE TIMING[3,5]					
Chip Select Write Width	t_{CS}		45	45	ns min
DAC Select Setup	t_{AS}		30	30	ns min
DAC Select Hold	t_{AH}		0	0	ns min
Data Setup	t_{DS}		30	15	ns min
Data Hold	t_{DH}		20	5	ns min
Load Setup	t_{LS}		20	20	ns min
Load Hold	t_{LH}		10	10	ns min
Load Pulse Width	t_{LDW}		30	30	ns min
Reset Pulse Width	t_{RS}		40	30	ns min
AC CHARACTERISTICS					
Output Slew Rate	SR	Data = 000_H to FFF_H to 000_H	0.05	0.05	V/µs typ
Settling Time[6]	t_S	To ±0.1% of Full Scale	70	60	µs typ
Shutdown Recovery Time	t_{SDR}			80	µs typ
DAC Glitch	Q	Code $7FF_H$ to 800_H to $7FF_H$	65	65	nVs typ
Digital Feedthrough	Q		15	15	nVs typ
Feedthrough	V_{OUT}/V_{REF}	V_{REF} = 1.5V_{DC} +1V_{P-P}, Data = 000_H, f=100KHz	–63	–63	dB typ
SUPPLY CHARACTERISTICS					
Power Supply Range	$V_{DD\ RANGE}$	DNL<±1LSB	2.7/5.5	2.7/5.5	V min/max
Positive Supply Current	I_{DD}	V_{IL} = 0V, No Load	--/200	--/200	µA typ/max
Shutdown Supply Current	I_{DD_SD}	SHDN=0, V_{IL} = 0V, No Load	0.1/1.5	0.1/1.5	µA typ/max
Power Dissipation	P_{DISS}	V_{IL} = 0V, No Load	600	1000	µW max
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%	0.003	0.006	%/% max

NOTES:

1. One LSB = V_{REF}/4096V for the 12-bit AD7396.
2. The first two codes (000_H, 001_H) are excluded from the linearity error measurement.
3. These parameters are guaranteed by design and not subject to production testing.
4. Typicals represent average readings measured at 25°C.
5. All input control signals are specified with $t_R = t_F$ = 2ns (10% to 90% of +3V) and timed from a voltage level of 1.6V.
6. The settling time specification does not apply for negative going transitions within the last 3 LSBs of ground.

AD7397 10-Bit ELECTRICAL CHARACTERISTICS at V_{REF}in = 2.5V, -40°C < T_A < +85°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	3V±10%	5V±10%	UNITS
STATIC PERFORMANCE					
Resolution[1]	N		10	10	Bits
Relative Accuracy[2]	INL	T_A = 25°C	±1.5	±1.5	LSB max
Relative Accuracy[2]	INL	T_A = -40°C, 85°C, 125°C	±2.0	±2.0	LSB max
Differential Nonlinearity[2]	DNL	Monotonic	±0.8	±0.8	LSB max
Zero-Scale Error	V_{ZSE}	Data = 000_H	9.0	9.0	mV max
Full-Scale Voltage Error	V_{FSE}	T_A = 25°C, 85°C, 125°C, Data = $3FF_H$	±32	±32	mV max
Full-Scale Voltage Error	V_{FSE}	T_A = -40°C, Data = $3FF_H$	±42	±42	mV max
Full-Scale Tempco[4]	TCV_{FS}		28	28	ppm/°C typ
REFERENCE INPUT					
V_{REF}in Range	V_{REF}		0/V_{DD}	0/V_{DD}	V min/max
Input Resistance	R_{REF}		2.5	2.5	MΩ typ[4]
Input Capacitance[3]	C_{REF}		5	5	pF typ
ANALOG OUTPUT					
Output Current (source)	I_{OUT}	Data = 200_H, ΔV_{OUT} = 5LSB	1	1	mA typ
Output Current (sink)	I_{OUT}	Data = 200_H, ΔV_{OUT} = 5LSB	3	3	mA typ
Capacitive Load[3]	C_L	No Oscillation	100	100	pF typ
LOGIC INPUTS					
Logic Input Low Voltage	V_{IL}		0.5	0.8	V min
Logic Input High Voltage	V_{IH}		V_{DD}-0.6	V_{DD}-0.6	V max
Input Leakage Current	I_{IL}		10	10	µA max
Input Capacitance[3]	C_{IL}		10	10	pF max
INTERFACE TIMING[3,5]					
Chip Select Write Width	t_{CS}		45	45	ns min
DAC Select Setup	t_{AS}		30	30	ns min
DAC Select Hold	t_{AH}		0	0	ns min
Data Setup	t_{DS}		30	15	ns min
Data Hold	t_{DH}		20	5	ns min
Load Setup	t_{LS}		20	20	ns min
Load Hold	t_{LH}		10	10	ns min
Load Pulse Width	t_{LDW}		30	30	ns min
Reset Pulse Width	t_{RS}		40	30	ns min
AC CHARACTERISTICS					
Output Slew Rate	SR	Data = 000_H to $3FF_H$ to 000_H	0.05	0.05	V/µs typ
Settling Time[6]	t_S	To ±0.1% of Full Scale	70	60	µs typ
Shutdown Recovery Time	t_{SDR}			80	µs typ
DAC Glitch	Q	Code $7FF_H$ to 800_H to $7FF_H$	65	65	nVs typ
Digital Feedthrough	Q		15	15	nVs typ
Feedthrough	V_{OUT}/V_{REF}	V_{REF} = $1.5V_{DC}$ +$1V_{P-P}$, Data = 000_H, f=100KHz	–63	–63	dB typ
SUPPLY CHARACTERISTICS					
Power Supply Range	$V_{DD\ RANGE}$	DNL<±1LSB	2.7/5.5	2.7/5.5	V min/max
Positive Supply Current	I_{DD}	V_{IL} = 0V, No Load	--/200	--/200	µA typ/max
Shutdown Supply Current	I_{DD_SD}	SHDN=0, V_{IL} = 0V, No Load	0.1/1.5	0.1/1.5	µA max
Power Dissipation	P_{DISS}	V_{IL} = 0V, No Load	600	1000	µW max
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%	0.003	0.006	%/% max

NOTES:

1. One LSB = V_{REF}/1024V for the 10-bit AD7397.
2. The first two codes (000_H, 001_H) are excluded from the linearity error measurement.
3. These parameters are guaranteed by design and not subject to production testing.
4. Typicals represent average readings measured at 25°C.
5. All input control signals are specified with $t_R = t_F$ = 2ns (10% to 90% of +3V) and timed from a voltage level of 1.6V.
6. The settling time specification does not apply for negative going transitions within the last 3 LSBs of ground.

ABSOLUTE MAXIMUM RATINGS

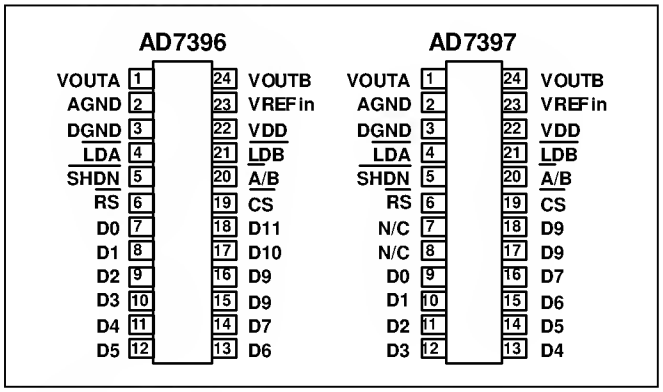
V_{DD} to GND .....–0.3V, +8V
VREF to GND .....–0.3V, V_{DD}
Logic Inputs to GND.....–0.3V, +8V
V_{OUT} to GND.....–0.3V, V_{DD} + 0.3V
AGND to DGND .....-0.3V, +2V
I_{OUT} Short Circuit to GND.....50mA
Package Power Dissipation ..... $(T_{J\ MAX} - T_A)/\theta_{JA}$
Thermal Resistance θ_{JA}
24-Pin Plastic DIP Package (N-24).....63°C/W
24-Lead SOIC Package (R-24).....70°C/W
24-Lead Thin-Shrink Surface Mount (RU-24).....143°C/W
Maximum Junction Temperature ($T_{J\ MAX}$)..... 150°C
Operating Temperature Range .....–40°C to +85°C
AD7397AR only.....–40°C to +125°C
Storage Temperature Range.....–65°C to +150°C
Lead Temperature:
N-24 (Soldering, 10 secs) ..... +300°C
R-24 (Vapor Phase, 60 secs)..... +215°C
RU-24 (Infrared, 15 secs)..... +224°C

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN DESCRIPTION

#	Name	Function
1	V_{OUTA}	DAC A voltage output.
2	AGND	Analog ground.
3	DGND	Digital ground.
4	LDA	Load DAC A register strobes. Transfers input register data to the DAC A register. Active low inputs, Level sensitive latch. May be connected together with LDB to double-buffer load both DAC registers simultaneously.
5	SHDN	Power Shutdown active low input. DAC register contents are saved as long as power stays on the V_{DD} pin.
6	RS	Resets DAC register to zero condition. Asynchronous active low input.
7-18	D0-D11	12 parallel input data bits. D11=MSB pin 18, D0=LSB pin 7, AD7396.
7,8	N/C	No connect pins 7 & 8 on the AD7397 only.
9-18	D0-D9	10 parallel input data bits. D9=MSB.pin 18, D0=LSB pin 9, AD7397 only.
19	CS	Chip Select latch enable, active low.
20	A/B	DAC register Address Select DACA=0 or DACB=1
21	LDB	Load DAC B register strobes. Transfers input register data to the DAC B register. Active low inputs, Level sensitive latch. May be connected together with LDA to double-buffer load both DAC registers simultaneously.
22	V_{DD}	Positive power supply input. Specified range of operation +2.7 to +5.5V.
23	V_{REFIN}	DAC reference input pin. Establishes DAC full-scale voltage.
24	V_{OUTB}	DAC B voltage output.

PIN CONFIGURATION



ORDERING GUIDE:

MODEL	RES (LSB)	TEMP	Package Description	Package Option
AD7396AN	12	-40/+85°C	24-pin P-DIP	N-24
AD7396AR	12	-40/+85°C	24-lead SOIC	R-24
AD7397AN	10	-40/+85°C	24-pin P-DIP	N-24
AD7397AR	10	-40/+125°C	24-lead SOIC	R-24
AD7397ARU	10	-40/+85°C	TSSOP-24	TSSOP-24

The AD7396/97 contains xxx transistors. The die size measures 90 mil X 107 mil = 9630 sq mil.

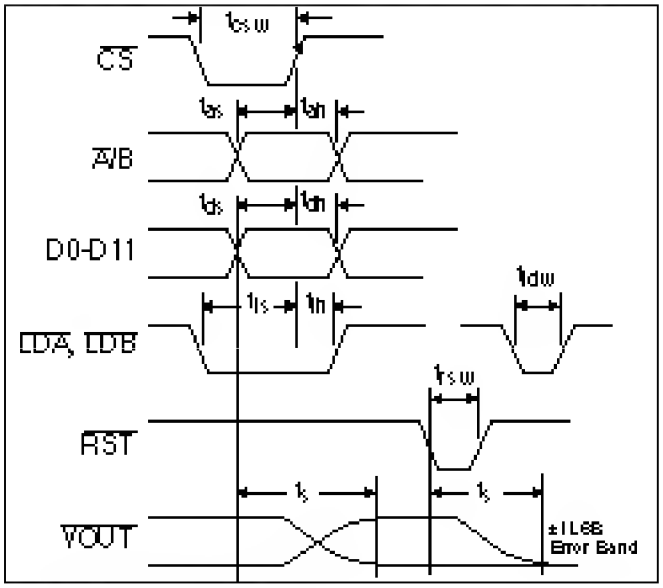


Figure 3. Timing Diagram

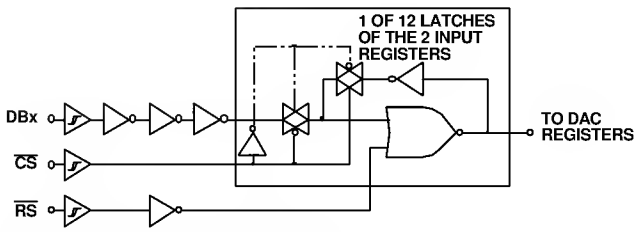


Figure 4. Digital Control Logic

Control Logic Truth Table

CS	A/B	LDA	LDB	RS	SHDN	Input Register	DAC Register
L	L	H	H	H	X	Write to A	Latched
L	H	H	H	H	X	Write to B	Latched
L	L	L	H	H	X	Write to A	A Transparent
L	H	H	L	H	X	Write to B	B Transparent
H	X	L	L	H	X	Latched	A & B Transparent
H	X	^	^	H	X	Latched	Latched
X	X	X	X	L	X	Reset to Zero Scale	Reset to Zero Scale
H	X	X	X	^	X	Latch Reset Value	Latch Reset Value

^ Denotes positive edge. The SHDN pin has no effect on the digital interface data loading; however, while in the SHDN state (SHDN=0) the output amplifiers V_{OUTA} & V_{OUTB} exhibit an open circuit conditon.

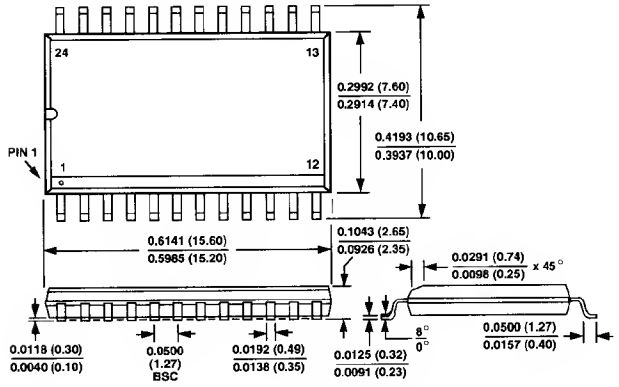
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7396/AD7397 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

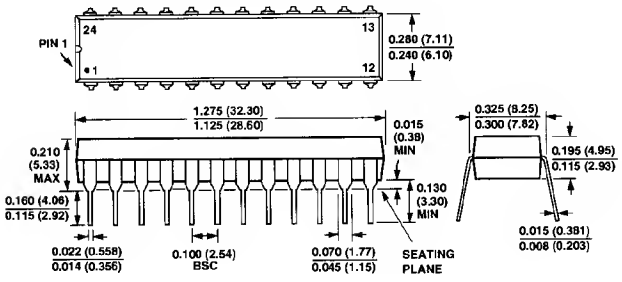
Mechanical Outline Dimensions

Dimensions shown in inches and (mm).

24-Pin SOIC Package (SOL-24)



24-Pin Narrow Body Plastic DIP Package (N-24)



24-Lead Thin Surface Mount TSSOP Package (RU-24)